Densitron

TFT DISPLAY MODULE

Product Specification

Customer	Standard	
Product Number	DMT050HDNMCMI-1A	
Customer Part Number		
Customer Approval		**Date:**

Internal Approvals		
Product Mgr	Doc. Control	Electr. Eng
Luo Luo	Filip Kaczorowski	Eric Wan
Date: 23/10/19	**Date: 23/10/19**	**Date: 23/10/19**

Revision Record

Rev.	Date	Page	Chapt.	Comment	ECR no.
1.0	23-Oct.-17	All	All	Initial Release	
1.1	23-Oct.-19	16	3.4.8	Updated timing values	

Table of Contents

1.0 Main Features

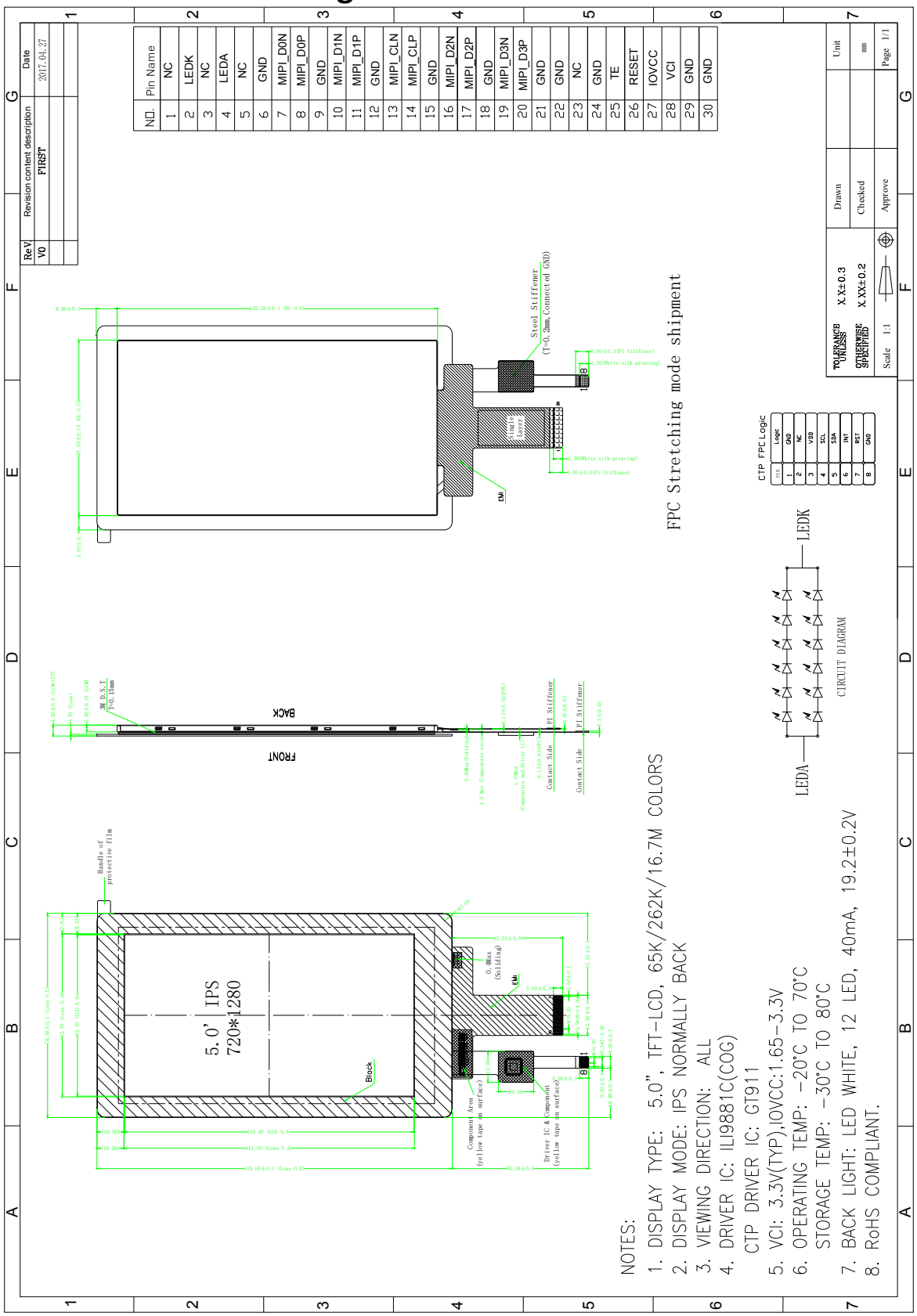
Item	Contents
Screen Size	5.0” Diagonal
Display Format	720 x RGB x 1280 Dots
N° of Colour	65K/262K/16.7M
Active Area	110.4 mm (V) x 62.1mm (H)
LCD Type	TFT
Mode	Transmissive / Normally Black
Viewing Direction	ALL
TFT Interface	4 Lane MIPI
PCT Interface	I2C
TFT Driver IC	ILI9881C
PCT Driver IC	GT911
Simultaneous Touch Points	5-point and Gestures
Backlight Type	LED
Operating Temperature	-20°C ~ +70°C
Storage Temperature	-30°C ~ +80°C
RoHS compliant	Yes

2.0 Mechanical Specification

2.1 Mechanical Characteristics

Item	Characteristic	Unit
Overall Dimensions	135.65mm (V) x 78.56mm (H) x 4.2 mm (D)	mm
pixel Pitch	86.25 (H) x 86.25 (V)	µm
Weight	75	g

2.2 Mechanical Drawing



3.0 Electrical Specification

3.1 Absolute Maximum Ratings

3.1 1 Absolute Maximum Ratings

Item	Symbol	Condition	Min	Max	Unit	Note
Power Supply Voltage LCM	VCI		-0.3	6.5	V	
Digital interface supply Voltage	IOVCC		-0.3	3.3	V	
Operating Temperature	T_{OP}		-20	70	°C	1
Storage Temperature	T_{ST}		-30	80	°C	1,2,3

Note 1. 90 % RH Max for Ta<50 °C, and 60% RH for Ta≥50°C.
Note 2. In case of below 0°C, the response time of liquid crystal (LC) becomes slower and the colour of panel becomes darker than normal one. Level of retardation depends on temperature, because of LC's characteristic.
Note 3. Only operation is guaranteed at operating temperature. Contrast, response time, another display quality are evaluated at +25°C.

3.1.2 PCT

Item	Symbol	Condition	Min	Max	Unit	Note
Power Supply Voltage	VDD	-	2.66	3.47	V	4
Operating Temperature	TOP	-	-20	70	°C	-
Storage Temperature	TST	-	-30	80	°C	-

3.2 Electrical Characteristics

3.2.1 TFT

Item	Symbol	Condition	Min	Typ	Max	Unit	Note
Supply Voltage	VCI	Ta=25˚C	2.5	3.3	6.0	V	
Digital interface supply Voltage	IOVCC	Ta=25˚C	1.65	1.8	3.3	V	
Input Voltage for Logic	VIH		0.7 IOVCC	-	IOVCC	V	
	VIL		-0.3	-	0.3 IOVCC	V	
Output Voltage for Logic	VOH		0.8 IOVCC	-	IOVCC	V	
	VOL		GND	-	0.2 IOVCC	V	
Current Consumption VCI	IDD		-	40	-	mA	
Current Consumption IOVCC	Icc			10		mA	

3.2.2 PCT

Item	Symbol	Condition	Min	Typ	Max	Unit	Note
Supply Voltage	VDD	Ta=25˚C	2.66	3.3	3.47	V	
Input Voltage for Logic	VIH		0.75 VDD	-	VDD +0.3	V	
	VIL		-0.3	-	0.25 VDD	V	
Output Voltage for Logic	VOH		0.85 VDD	-	-	V	
	VOL		-	-	0.15 VDD	V	
Normal operation mode Current	IOPR		-	8	14.5	mA	
Green mode Current Consumption	IMON		-	3.3	-	mA	
Sleep mode Current Consumption	ISLP		70	-	120	uA	
Doze mode Current Consumption	IDOZ		-	0.78	-	mA	

3.3 Interface Pin Assignment

3.3.1 TFT Pin Assignment

No.	Symbol	Function
1	NC	Not Connected
2	LEDK	Cathode pin of backlight
3	NC	Not Connected
4	LEDA	Anode pin of backlight.
5	NC	Not Connected
6	GND	Ground
7	MIPI_D0N	MIPI DSI differential data pair. (Data lane 0)
8	MIPI_D0P	
9	GND	Ground
10	MIPI_D1N	MIPI DSI differential data pair. (Data lane 1)
11	MIPI_D1P	
12	GND	Ground
13	MIPI_CLN	MIPI DSI differential clock pair。
14	MIPI_CLP	
15	GND	Ground
16	MIPI_D2N	MIPI DSI differential data pair. (Data lane 2)
17	MIPI_D2P	
18	GND	Ground
19	MIPI_D3N	MIPI DSI differential data pair. (Data lane 3)
20	MIPI_D3P	
21	GND	Ground
22	GND	Ground
23	NC	Not Connected
24	GND	Ground
25	TE	Tearing effect output pin. Leave the pin open when not in use
26	RESET	- The external reset input Initializes the chip with a low input. Be sure to execute a p

No.	Symbol	Function
		ower-on reset aftersupplying power. Fix to IOVCC level when not in use.
27	IOVCC	- Power supply for internal logic regulator. Connect to an external power supply of 1.65V to 3.3V
28	VCI	- Power supply for analog circuits. Connect to an external power supply of 2.8V to 3.3V
29	GND	Ground
30	GND	Ground

3.3.2 PCT PIN ASSIGNMENT

No.	Symbol	Function
1	GND	Ground
2	NC	Not Connected
3	VDD	Supply voltage
4	SCL	I2C clock input
5	SDA	I2C data input and output
6	INT	External interrupt to the host
7	RST	External Reset, Low is active
8	GND	Ground.

3.4 MIPI Interface Characteristics

3.4.1 High Speed Mode – Clock Channel Timing

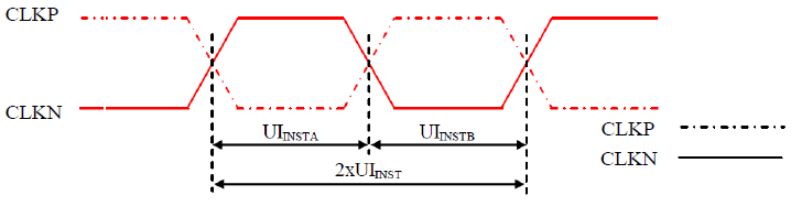


Figure 118: DSI Clock Channel Timing

Table 38: DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N	$2xUI_{INST}$	Double UI instantaneous	4	25	ns
CLKP/N	UI_{INSTA},UI_{INSTB} (Note 1)	UI instantaneous Half	2 (Note 2)	12.5	ns

Notes:

1. UI = UIINSTA = UIINSTB

2. Define the minimum value of 24 UI per Pixel, see Table 39.

Table 39: Limited Clock Channel Speed

Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	566 Mbps	433 Mbps	366 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	637 Mbps	487 Mbps	412 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	850 Mbps	650 Mbps	550 Mbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	850 Mbps	650 Mbps	550 Mbps

3.4.2 High Speed Mode – Data Clock Channel Timing

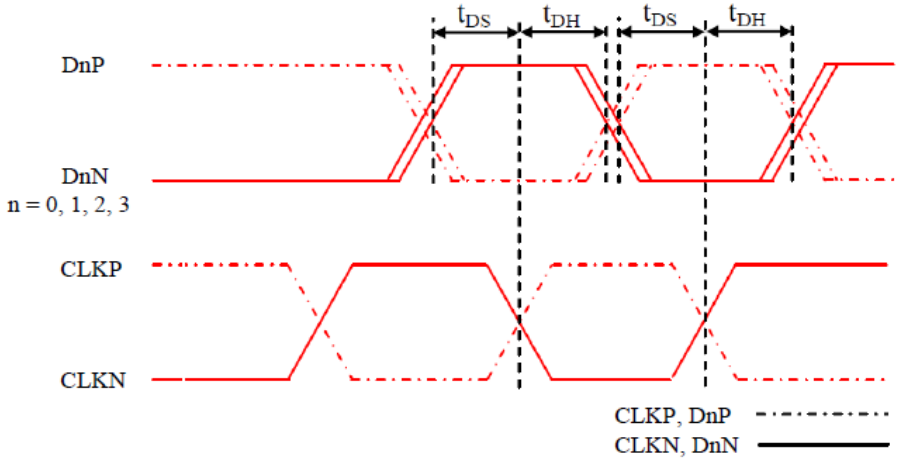


Figure 119: DSI Data to Clock Channel Timings

Table 40: DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DnP/N , n=0 and 1	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

3.4.3 High Speed Mode – Rising and Fall Timings

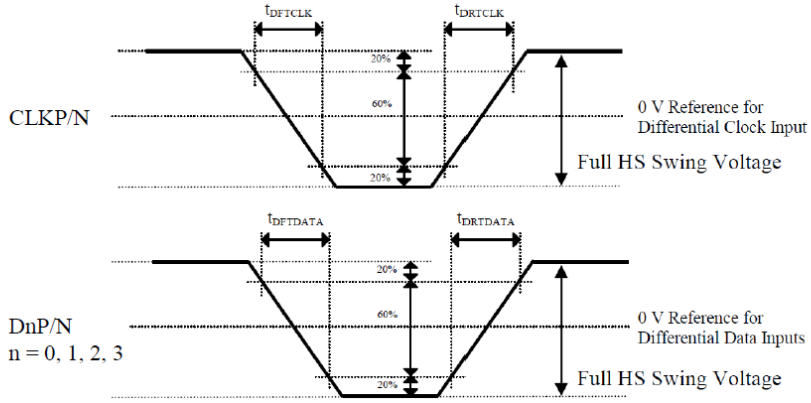


Figure 120: Rising and Falling Timings on Clock and Data Channels

Table 41: Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification		
			Min	Typ	Max
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)

Note: *The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.*

3.4.4 Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the MCU to the Display Module (ILI9881C) are illustrated for reference purposes below.

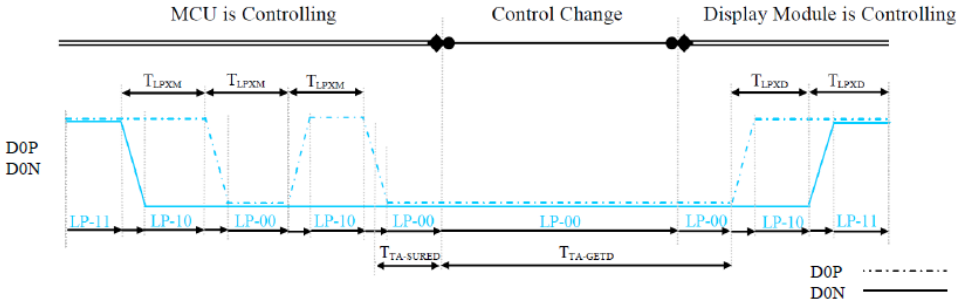


Figure 121: BTA from the MCU to the Display Module

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the Display Module (ILI9881C) to the MCU are illustrated for reference purposes below.

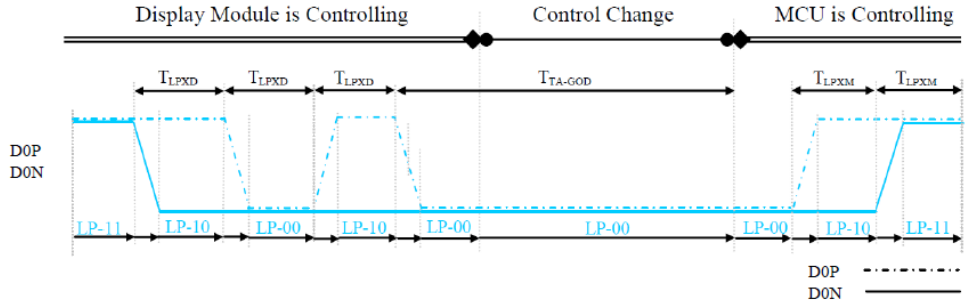


Figure 122: BTA from the Display Module to the MCU

Table 42: Low Power State Period Timings – A

Signal	Symbol	Description	Min	Max	Unit
D0P/N	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU ➔ Display Module (ILI9881C)	50	75	ns
D0P/N	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9881C) ➔ MCU	50	75	ns
D0P/N	$T_{TA-SURED}$	Time-out before the Display Module (ILI9881C) starts driving	T_{LPXD}	$2xT_{LPXD}$	ns

Table 43: Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
D0P/N	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (ILI9881C)	$5xT_{LPXD}$	ns
D0P/N	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MCU	$4xT_{LPXD}$	ns

3.4.5 Data Lanes from Low Power Mode to High Speed Mode

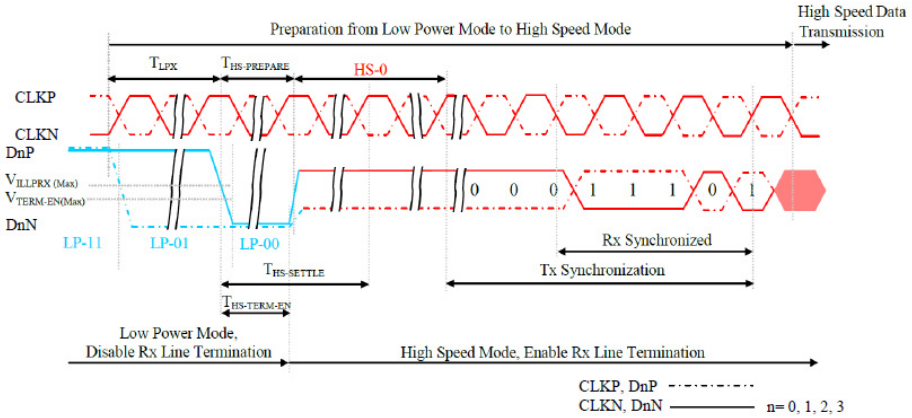


Figure 123: Data Lanes - Low Power Mode to High Speed Mode Timings

Table 44: Data Lanes - Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	T_{LPX}	Length of any Low Power State Period	50	-	ns
DnP/N, n = 0 and 1	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DnP/N, n = 0 and 1	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

3.4.6 Data Lanes from High Power Mode to High Speed Mode

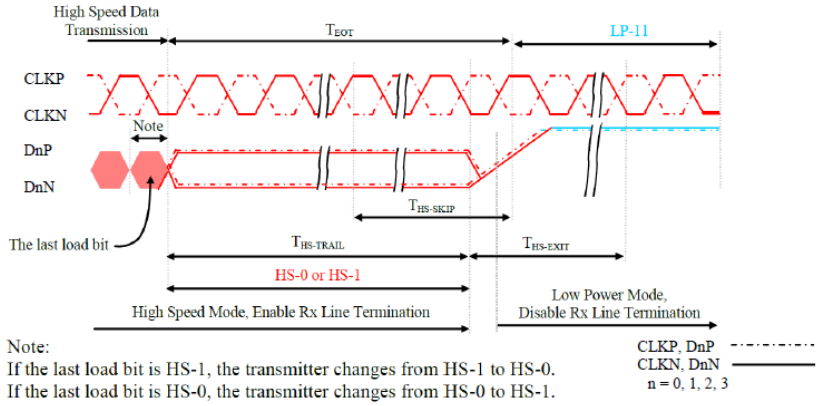


Figure 124: Data Lanes - High Speed Mode to Low Power Mode Timings

Table 45: Data Lanes - High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	$T_{HS-SKIP}$	Time-Out at Display Module (ILI9881C) to ignore transition period of EoT	40	55+4xUI	ns
DnP/N, n = 0 and 1	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

3.4.7 DSI Clock Burst – High Speed Mode to/from Low Power Mode

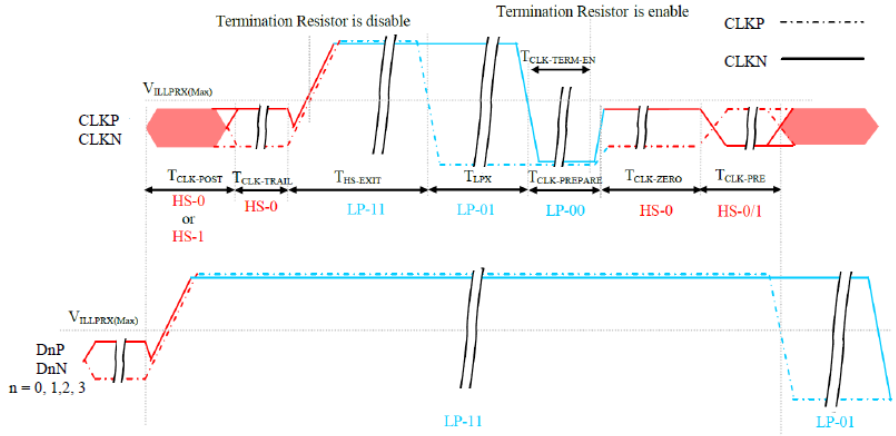


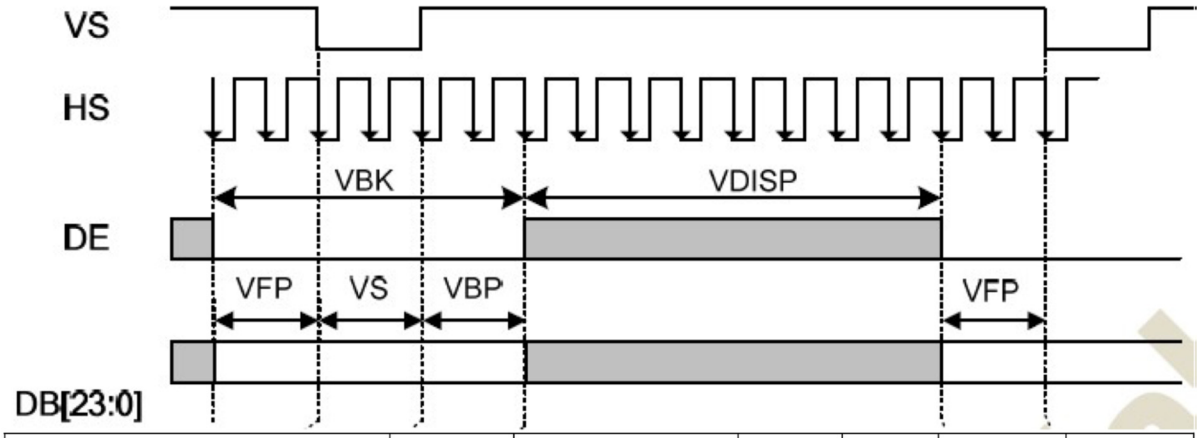
Figure 125: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Table 46: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
CLKP/N	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
CLKP/N	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
CLKP/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
CLKP/N	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
CLKP/N	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
CLKP/N	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
CLKP/N	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

3.4.8 Timing for DSI video mode

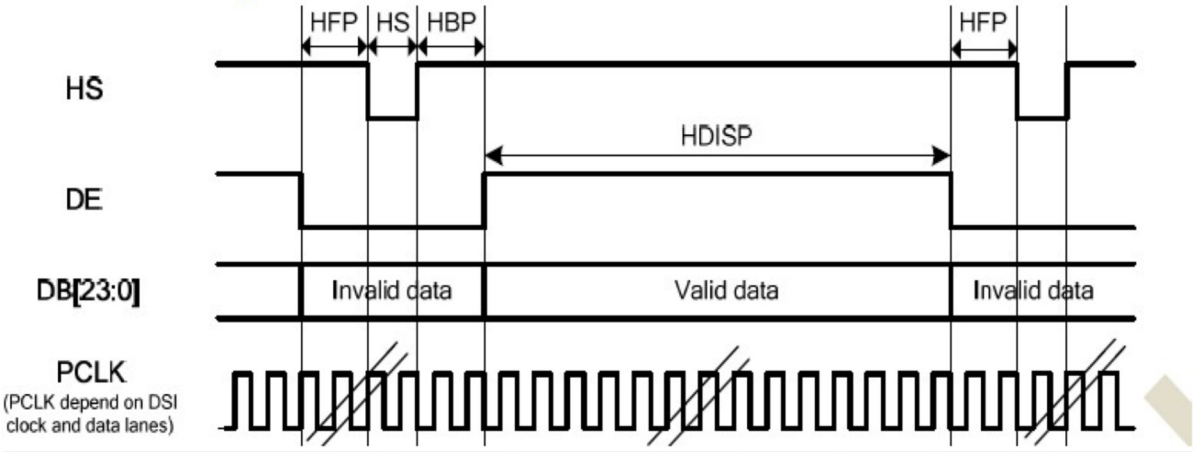
- Vertical Timings



Item	Symbol	Condition	Min	Typ	Max.	Unit
Vertical low pulse width	VS	--	2	(4)	Note(1)	Line
Vertical front porch	VFP	--	2	(10)	--	Line
Vertical back porch	VBP	--	6	(20)	Note(1)	Line
Vertical blanking period	VBK	VS+VBP+VFP	--	(34)	--	Line
Vertical active area	-	VDISP	--	1280	--	Line
Vertical Refresh rate	VRR	--	--	60	--	HZ

Note: The VS and VBP pulse width are related to GIP start pulse and GIP clock pulse timing. The GIP start pulse and GIP clock pulse must be set at correstponding position for LCD normal display.

- Horizontal Timings



Item	Symbol	Condition	Min	Typ	Max.	Unit
HS low pulse width	HS	--	6	(6)	78	DCK
Horizontal front porch	HFP	--	5	(10)	78	DCK
Horizontal back porch	HBP	--	5	(20)	78	DCK
Horizontal blanking period	HBK	HS+HBP+HFP	--	(36)	88	DCK
Horizontal active area	-	HDISP	--	720	--	DCK

3.4.9 Reset input timing

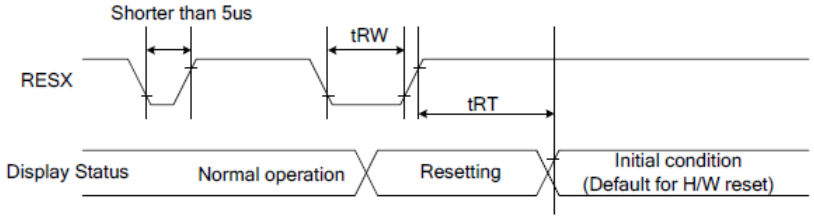


Figure 126: Reset Timing

Table 47: Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

Notes:

1. *The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.*
2. *Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 48.*

Table 48: Reset Descript

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

3. During the Resetting period, the display will be blanked (The display enters the blanking sequence, which maximum time is 120 ms, when Reset Starts in the Sleep Out mode. The display remains the blank state in the Sleep In mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection can also be applied during a valid reset pulse, as shown below:

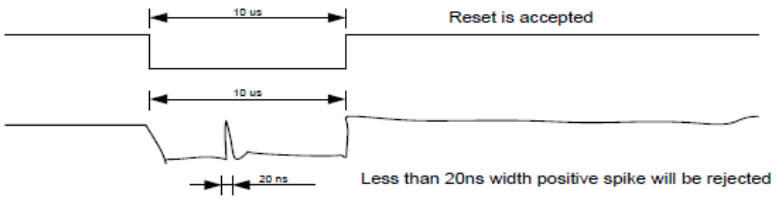
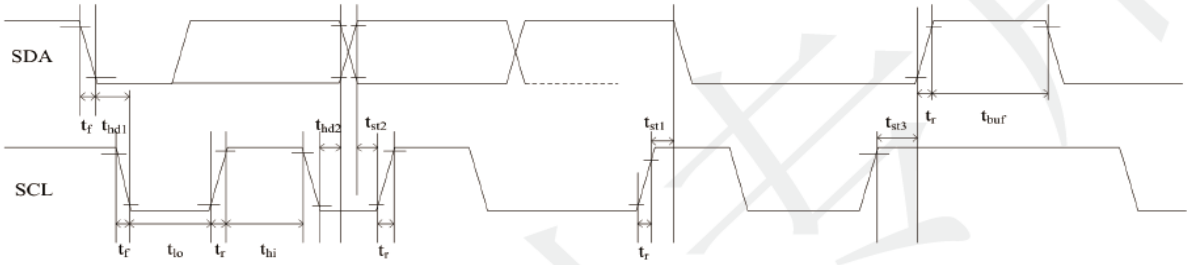


Figure 127: Positive Noise Pulse during Reset Low

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

3.4.10 I2C Timing

GT911 provides a standard I2C interface for SCL and SDA to communicate with the host. GT911 always serves as slave device in the system with all communication being initialized by the host.It is strongly recommended that transmission rate be kept at or below 400Kbps. The I2C timing is shown below:



Test condition 1: 1.8V host interface voltage, 400Kbps transmission rate, 2K pull-up resistor

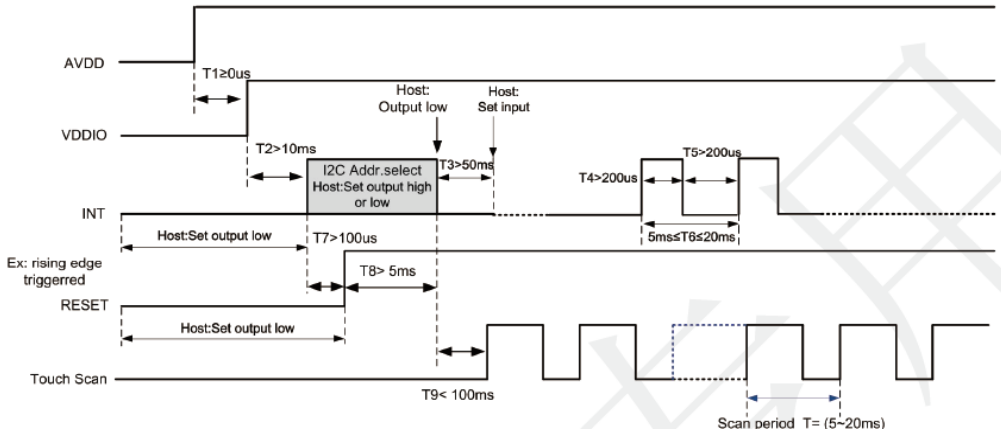
Parameter	Symbol	Min.	Max.	Unit
SCL low period	t_{lo}	1.3	-	us
SCL high period	t_{hi}	0.6	-	us
SCL setup time for Start condition	t_{st1}	0.6	-	us
SCL setup time for Stop condition	t_{st3}	0.6	-	us
SCL hold time for Start condition	t_{hd1}	0.6	-	us
SDA setup time	t_{st2}	0.1	-	us
SDA hold time	t_{hd2}	0	-	us

Test condition 2: 3.3V host interface voltage, 400Kbps transmission rate, 2K pull-up resistor

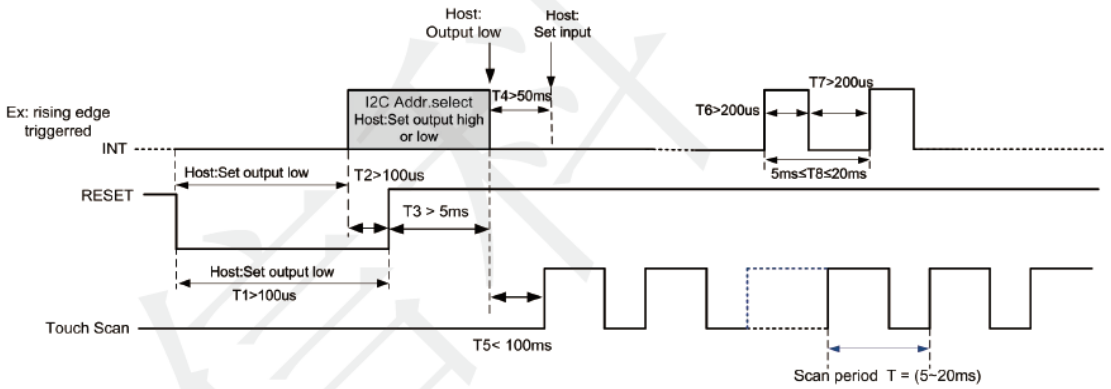
Parameter	Symbol	Min.	Max.	Unit
SCL low period	t_{lo}	1.3	-	us
SCL high period	t_{hi}	0.6	-	us
SCL setup time for Start condition	t_{st1}	0.6	-	us
SCL setup time for Stop condition	t_{st3}	0.6	-	us
SCL hold time for Start condition	t_{hd1}	0.6	-	us
SDA setup time	t_{st2}	0.1	-	us
SDA hold time	t_{hd2}	0	-	us

GT911 supports two I2C slave addresses: 0xBA/0xBB and 0x28/0x29. The host can select the address by changing the status of Reset and INT pins during the power-on initialization phase. See the diagram below for configuration methods and timings:

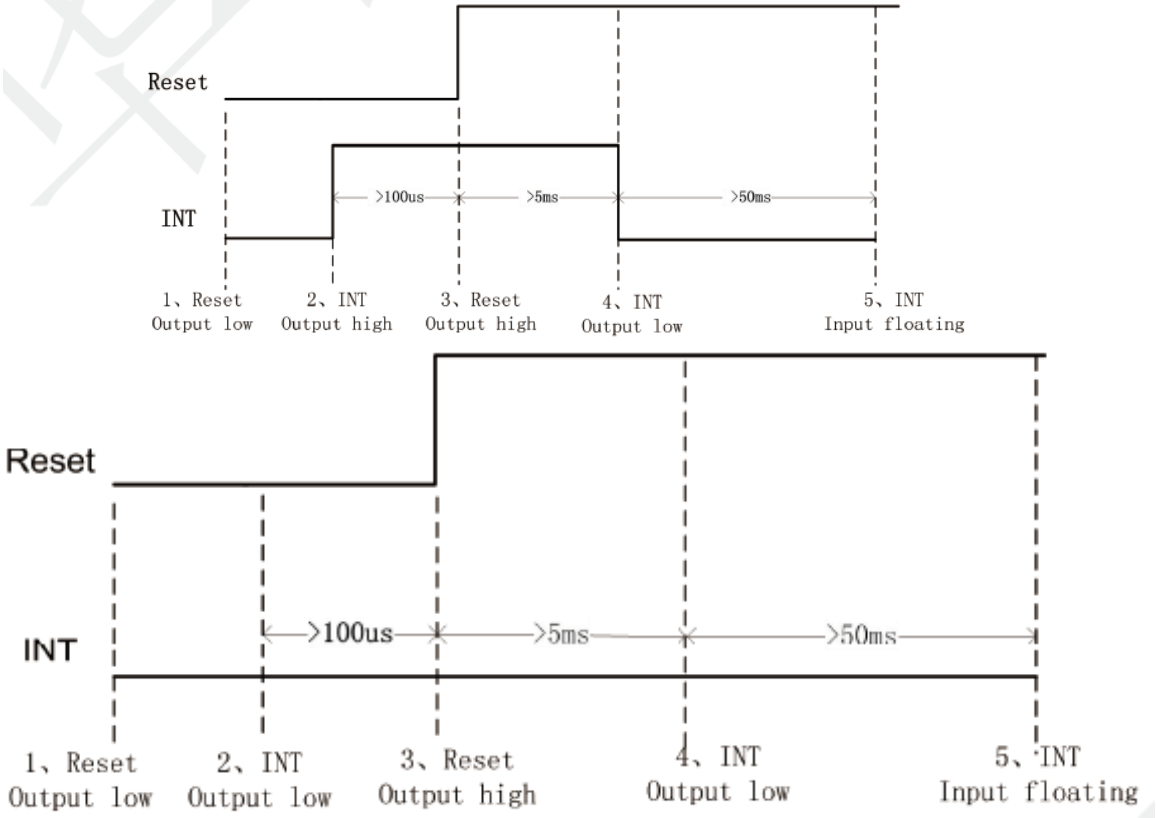
Power-on Timing:



Timing for host resetting GT911:



Timing for setting slave address to 0x28/0x29:



a) Data Transmission

(For example：device address is 0xBA/0xBB)

Communication is always initiated by the host. Valid Start condition is signaled by pulling SDA line from “high” to “low” when SCL line is “high”. Data flow or address is transmitted after the Start condition.

All slave devices connected to I^2C bus should detect the 8-bit address issued after Start condition and send the correct ACK. After receiving matching address, GT911 acknowledges by configuring SDA line as output port and pulling SDA line low during the ninth SCL cycle. When receiving unmatched address, namely, not 0XBA or 0XBB, GT911 will stay in an idle state.

For data bytes on SDA, each of 9 serial bits will be sent on nine SCL cycles. Each data byte consists of 8 valid data bits and one ACK or NACK bit sent by the recipient. The data transmission is valid when SCL line is “high”.

When communication is completed, the host will issue the STOP condition. Stop condition implies the transition of SDA line from “low” to “high” when SCL line is “high”.

b) Writing Data to GT911

(For example：device address is 0xBA/0xBB)

Timing for Write Operation

The diagram above displays the timing sequence of the host writing data onto GT911. First, the host issues a Start condition. Then, the host sends 0XBA (address bits and R/W bit; R/W bit as 0 indicates Write operation) to the slave device.

After receiving ACK, the host sends the 16-bit register address (where writing starts) and the 8-bit data bytes (to be written onto the register).

The location of the register address pointer will automatically add 1 after every Write Operation. Therefore, when the host needs to perform Write Operations on a group of registers of continuous addresses, it is able to write continuously. The Write Operation is terminated when the host issues the Stop condition.

c) Reading Data from GT911

(For example：device address is 0xBA/0xBB)

Timing for Read Operation

The diagram above is the timing sequence of the host reading data from GT911. First, the host issues a Start condition and sends 0XBA (address bits and R/W bit; R/W bit as 0 indicates Write operation) to the slave device.

After receiving ACK, the host sends the 16-bit register address (where reading starts) to the slave device. Then the host sets register addresses which need to be read.

Also after receiving ACK, the host issues the Start condition once again and sends 0XBB (Read Operation). After receiving ACK, the host starts to read data.

GT911 also supports continuous Read Operation and, by default, reads data continuously. Whenever receiving a byte of data, the host sends an ACK signal indicating successful reception. After receiving the last byte of data, the host sends a NACK signal followed by a STOP condition which terminates communication.

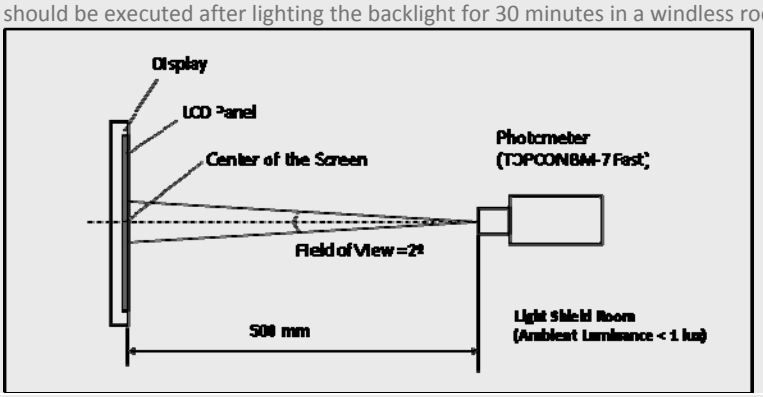
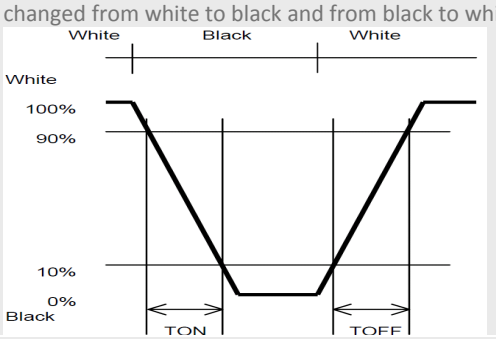
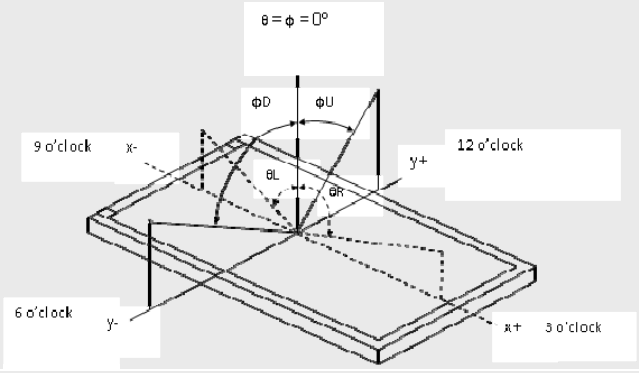
4.0 Optical Specification

4.1 Optical Characteristics

Measuring instruments ： LCD-5100, Eldim, Topcon BM-7
Driving condition: VCI = 3.3V, VSS = 0V
Backlight: IF=40mA
Measured temperature: Ta ＝ 25 ˚C

Item		Symbol	Condition	Min	Typ	Max	Unit	Note
Response Time		TR+TF	θ=Φ=0° Normal Viewing Angle	-	30	40	ms	2
Contrast Ratio		CR		640	800	-		3
Viewing Angle	Left	θL	CR ≥ 10	-	80	-	deg	4
	Right	θR		-	80	-	deg	
	Up	ϕU		-	80	-	deg	
	Down	ϕD		-	80	-	deg	
Colour Chromaticity	Red	Rx	CR ≥ 10	0.611	0.631	0.651	-	5
		Ry		0.319	0.339	0.359	-	
	Green	Gx		0.300	0.320	0.340	-	
		Gy		0.587	0.607	0.627	-	
	Blue	Bx		0.131	0.151	0.171	-	
		By		0.025	0.045	0.065	-	
	White	Wx		0.276	0.316	0.356	-	
		Wy		0.296	0.336	0.376	-	
Centre Brightness				380	420	-	cd/m²	6
Brightness Distribution				80	-	-	%	7

4.1.1 Test Method

Note	Item	Test Method
1	Setup	The display should be stabilised at a given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilise the luminance, measurements should be executed after lighting the backlight for 30 minutes in a windless room. 
2	Response time	Measure output signal waveform by the luminance meter when raster of window pattern is changed from white to black and from black to white. 
3	Contrast ratio	Measure maximum brightness and minimum brightness at the centre of the screen by displaying raster or window pattern. Then calculate the ratio between these two values. Contrast Ratio (CR) = Brightness of unselected position (white) / Brightness of selected position (black)
4	Viewing angle Horizontal θ Vertical Ø	Move the luminance meter from right to left and up and down and determinate the angles where contrast ratio is 10 
5	Colour chromaticity	Measure chromaticity coordinates x and y of CIE1931 colorimetric system
6	Centre brightness	Measure the brightness at the centre of the screen
7	Brightness distribution	(Brightness distribution) = 100 x B/A % A: max. brightness of the 9 points B: min. brightness of the 9 points

5.0 Backlight Specification

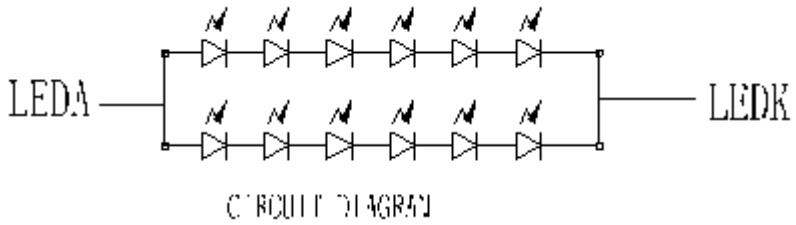
5.1 LED Driving Conditions

Item	Symbol	Condition	Min	Typ	Max	Unit
Forward Current	IF	Ta=25 °C	30	40	-	mA
Forward Voltage	VF	Ta= 25°C		19.2		V
LED life time	Hr				50k	hour

Note:

- The lifetime of the LED is defined as a period till the brightness of the LED decreases to the half of its initial value.
- This figure is given as a reference purpose only, and not a guarantee.
- This figure is estimated for an LED operating alone.
  The performance of an LED may differ when assembled as a monitor together with a TFT panel due to different environmental temperature.
- Estimated lifetime could vary on a different temperature and usually higher temperature could reduce the life significantly.

5.2 LED Circuit



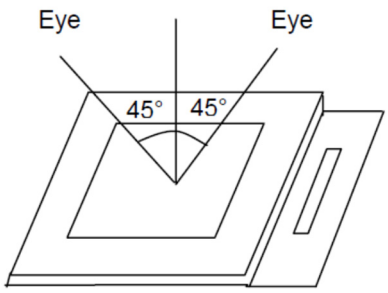
LED Circuit Drawing

6.0 Quality Assurance Specification

6.1 Delivery Inspection Standards

6.1.1 Inspection Conditions

Inspection distance: 30 cm ± 2 cm
Viewing angle: ±45°



6.1.2 Environmental Conditions

Ambient temperature: 25°C ±5°C
Ambient humidity: 65±10% RH
Ambient illumination: 300~700 lux

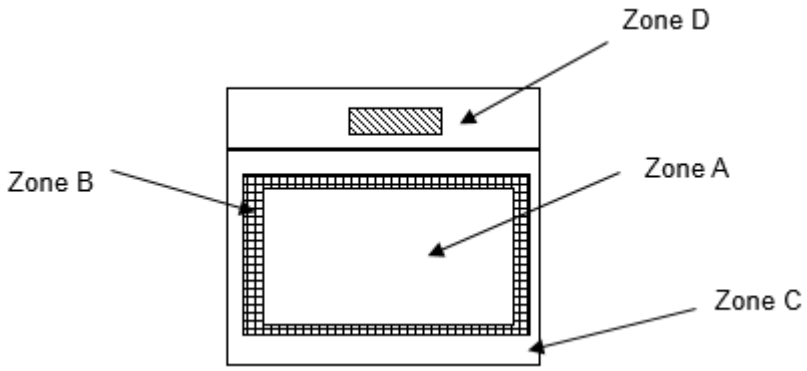
6.1.3 Sampling Conditions

1. Lot size: quantity of shipment lot per model
2. Sampling method:

Sampling Plan		GB/T 2828-2003
		Normal inspection, Class II
AQL	Major Defect	0.65%
	Minor Defect	1.5%

No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. 4) TP no function	Major
2	Missing	Missing component	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Spot Line defect	Light dot , Dim spot,Polarizer Bubble ; Polarizer accidented spot.	
6	Soldering appearance	Good soldering , Peeling off is not allowed.	

6.1.4 Definition of Area

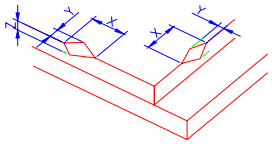
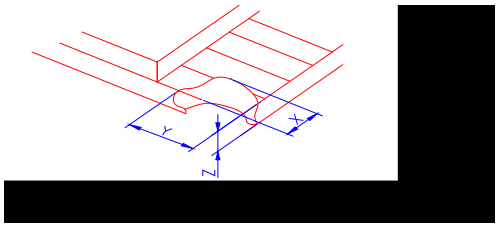
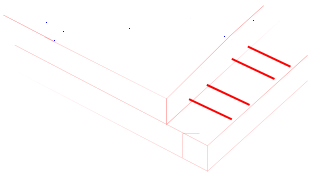


Zone A : Effective Viewing Area(Character or Digit can be seen)
Zone B : Viewing Area except Zone A
Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer .)
Zone D : IC Bonding Area
Note:
As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer

6.1.5 Basic Principle

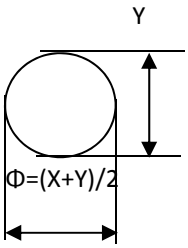
A set of sample to indicate the limit of acceptable quality level shall be discussed should a dispute occur.

6.1.6 Inspection Criteria

<table>
<tr><th>Number</th><th>Items</th><th>Criteria(mm)</th></tr>
<tr><td rowspan="3">1.0 LCD Crack/Broken
NOTE:
X: Length
Y: Width
Z: Height
L: Length of ITO
T: Height of LCD</td><td>(1) The edge of LCD broken</td><td> 
<table>
<tr><td>X</td><td>Y</td><td>Z</td></tr>
<tr><td>≤3.0mm</td><td><Inner border line of the seal</td><td>≤T</td></tr>
</table></td></tr>
<tr><td>(2)LCD corner broken</td><td> 
<table>
<tr><td>X</td><td>Y</td><td>Z</td></tr>
<tr><td>≤3.0mm</td><td>≤L</td><td>≤T</td></tr>
</table></td></tr>
<tr><td>(3)LCD crack</td><td> 
Crack
Not allowed</td></tr>
</table>

2.0

Spot defect



① light dot （LCD/TP/Polarizer black/white spot , light dot, pinhole, dent, stain）

Size (mm) \ Zone	Acceptable Qty		
	A	B	C
Φ≤0.10	Ignore		Ignore
0.10<Φ≤0.25	4(distance≧10mm)		
0.25<Φ≤0.35	3		
Φ>0.4	0		

②Dim spot （LCD/TP/Polarizer dim dot, light leakage、 dark spot）

Size (mm) \ Zone	Acceptable Qty		
	A	B	C
Φ≤0.1	Ignore		Ignore
0.10<Φ≤0.25	4(distance≧10mm)		
0.25<Φ≤0.35	3		
Φ>0.4	0		

③ Polarizer accidented spot

Size (mm) \ Zone	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.3<Φ≤0.5	3(distance≧10mm)		
Φ>0.5	1		

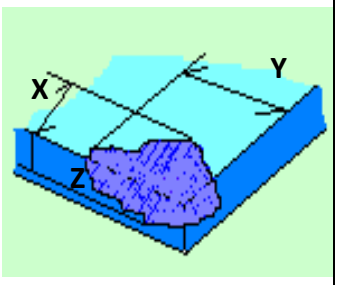
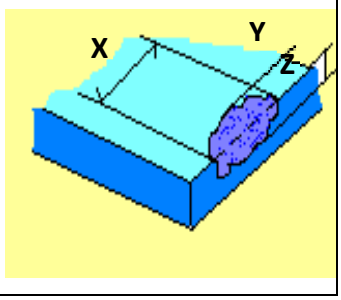
④Pixel bad points （light dot， Dim dot, color dot）

Size (mm) \ Zone	Acceptable Qty		
	A	B	C
Φ≤0.15	Ignore		Ignore
0.2<Φ≤0.3	2(distance≧10mm)		
Φ>0.4	1		

⑤ Polarizer Bubble

Size (mm) \ Zone	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.3<Φ≤0.4	4(distance≧10m)		
0.4<Φ≤0.5	3		
Φ>0.5	1		

<table>
<tr><td>3.0</td><td>Line defect (LCD/TP/Polarizer backlight black/white line, scratch, stain)</td><td colspan="2">
<table>
<tr><td rowspan="2">Width(mm)</td><td rowspan="2">Length(mm)</td><td colspan="3">Acceptable Qty</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>Φ≤0.05</td><td>Ignore</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.05<W≤0.06</td><td>L≤4.0</td><td colspan="2">N≤3</td></tr>
<tr><td>0.07<W≤0.08</td><td>L≤3.0</td><td colspan="2">N≤2</td></tr>
<tr><td>0.08<W</td><td colspan="4">Define as spot defect</td></tr>
</table>
</td></tr>
<tr><td>4.0</td><td>Electronic Components SMT</td><td colspan="2">Not allow missing parts, solderless connection, cold solder joint, mismatch, The positive and negative polarity opposite</td></tr>
<tr><td>5.0</td><td>Display color & Brightness</td><td colspan="2">1. Color：Measuring the color coordinates, The measurement standard according to the datasheet or samples.
2. Brightness：Measuring the brightness of White screen, The measurement standard according to the datasheet or Samples.</td></tr>
<tr><td rowspan="4">6.0</td><td rowspan="4">PCT Related</td><td>PCT Cover sensor accidented black/white spot</td><td>
<table>
<tr><td rowspan="2">Size Φ(mm)</td><td colspan="3">Acceptable Qty</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>Φ≤0.1</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.15<Φ≤0.25</td><td colspan="2">4（distance≧10mm）</td></tr>
<tr><td>0.25<Φ≤0.35</td><td colspan="2">3</td></tr>
<tr><td>Φ>0.4</td><td colspan="2">1</td><td></td></tr>
</table>
</td></tr>
<tr><td>PCT Cover scratch</td><td>
<table>
<tr><td rowspan="2">Width(mm)</td><td rowspan="2">Ignore(mm)</td><td colspan="3">Acceptable Qty</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>Φ≤0.05</td><td>Ignore</td><td colspan="3">Ignore</td></tr>
<tr><td>0.05<W≤0.06</td><td>L≤4.0</td><td colspan="3">N≤3</td></tr>
<tr><td>0.07<W≤0.08</td><td>L≤3.0</td><td colspan="3">N≤2</td></tr>
<tr><td>0.08<W</td><td colspan="4">Define as spot defect</td></tr>
</table>
</td></tr>
<tr><td>PCT Cover Pinhole/ Lack of ink</td><td>
<table>
<tr><td>Zone / Size (mm)</td><td>Acceptable Qty</td></tr>
<tr><td></td><td>C</td></tr>
<tr><td>Φ≤0.2</td><td>Ignore</td></tr>
<tr><td>0.2<Φ≤0.3</td><td>4(distance≧10mm)</td></tr>
<tr><td>0.3<Φ≤0.4</td><td>3</td></tr>
<tr><td>Φ>0.4</td><td>0</td></tr>
</table>
</td></tr>
<tr><td>PCT Bonding bubble/ accidented spot</td><td>
<table>
<tr><td rowspan="2">Size Φ(mm)</td><td colspan="2">Acceptable Qty</td></tr>
<tr><td>A</td><td>B</td></tr>
<tr><td>Φ≤0.1</td><td colspan="2">Ignore</td></tr>
<tr><td>0.15<Φ≤0.2</td><td colspan="2">3(distance≧10mm）</td></tr>
<tr><td>0.2<Φ≤0.25</td><td colspan="2">2</td></tr>
<tr><td>Φ>0.25</td><td colspan="2">0</td></tr>
</table>
</td></tr>
<tr><td>Assembly deflection</td><td>beyond the edge of backlight ≤0.2mm</td></tr>
</table>

<table>
<tr>
<td></td>
<td></td>
<td>TP cover broken
X：length
Y：width
Z：height</td>
<td>
<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>X≤0.5mm</td><td>Y≤0.5mm</td><td>Z<cover thickness</td></tr>
</table>
*Circuitry broken is not allowed.
</td>
<td> 
</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TP cover broken
X：length
Y：width
Z：height</td>
<td>
<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>X≤0.3mm</td><td>Y≤0.3mm</td><td>Z<LCD thickness</td></tr>
</table>
* Circuitry broken is not allowed.
</td>
<td> 
</td>
</tr>
</table>

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed
5	TP no function	Not allowed

6.1.7 Classification of Defects

Visual defects (except no or wrong label) are treated as minor defects, while electrical defects are treated as major defects.
Two minor defects are equal to one major defect in lot sampling inspection.

6.1.8 Identification / marking criteria

Any unit with illegible / wrong / double or no marking / label shall be rejected.

6.2 Dealing with Customer Complaints

6.2.1 Non-conforming analysis

Purchaser should supply Densitron with detailed data of non-conforming sample.
After accepting it, Densitron should complete the analysis in two weeks from receiving the sample.
If the analysis cannot be completed on time, Densitron must inform the purchaser.

6.2.2 Handling of non-conforming displays

If any non-conforming displays are found during customer acceptance inspection which Densitron is clearly responsible for, return them to Densitron.
Both Densitron and customer should analyse the reason and discuss the handling of non-conforming displays when the reason is not clear.
Equally, both sides should discuss and come to agreement for issues pertaining to modification of Densitron quality assurance standard.

7.0 Reliability Specification

7.1 Reliability Tests

Test Item		Test Condition		Inspection after test
Durability Test	High Temperature Operating	70℃	96h	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1.Air bubble in the LCD; 2.Non-display; 3.Missing segments/line; 4.Glass crack; 5.Current IDD is twice higher than initial value.
	Low Temperature Operating	-20℃	96h	
	High Temperature Storage	80℃	96h	
	Low Temperature Storage	-30℃	96h	
	High Temperature & Humidity Storage	+60℃, 90% RH ,96 hours.		
	Thermal Shock (Non-operation)	-30℃,30 min ↔ 80℃,30 min, Change time:5min 20CYC.		
	ESD Test	C=150pF,R=330Ω,5points/panel,Air:±8KV, 5times; Contact:±6KV, 5 times; (Environment: 15℃~35℃, 30%~60%).		
	Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total) (Package condition).		
	Box Drop Test	1 Corner 3 Edges 6 faces, 80 cm (Medium Box)		

Note: Ta=ambient temperature Tp= Panel temperature

Notes:
1.The test samples should be applied to only one test item.
2.Sample size for each test item is 5~10pcs.
3.For Damp Proof Test, Pure water(Resistance＞10MΩ) should be used.
4.In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.
5.Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

8.0 Handling Precautions

Safety

If the LCD panel breaks, be careful not to get the liquid crystal fluid in your mouth or in your eyes.
If the liquid crystal touches your skin or clothes, wash it off immediately using soap and plenty of water.

Mounting and Design

Place a transparent plate (e.g. acrylic, polycarbonate or glass) on the display surface to protect the display from external pressure. Leave a small gap between the transparent plate and the display surface.
When assembling with a zebra connector, clean the surface of the pads with alcohol and keep the surrounding air very clean.
Design the system so that no input signal is given unless the power supply voltage is applied.

Caution during LCD cleaning

Lightly wipe the display surface with a soft cloth soaked with Isopropyl alcohol, Ethyl alcohol or Trichlorotriflorothane.
Do not wipe the display surface with dry or hard materials that will damage the polariser surface.
Do not use aromatic solvents (toluene and xylene), or ketonic solvents (ketone and acetone).

Caution against static charge

As the display uses C-MOS LSI drivers, connect any unused input terminal to VDD or VSS. Do not input any signals before power is turned on. Also, ground your body, work/assembly table and assembly equipment to protect against static electricity.

Packaging

Displays use LCD elements, and must be treated as such. Avoid strong shock and drop from a height. To prevent displays from degradation, do not operate or store them exposed directly to sunshine or high temperature/humidity.

Caution during operation

It is indispensable to drive the display within the specified voltage limit since excessive voltage shortens its life. Direct current causes an electrochemical reaction with remarkable deterioration of the display quality. Give careful consideration to prevent direct current during ON/OFF timing and during operation. Response time is extremely delayed at temperatures lower than the operating temperature range while, at high temperatures, displays become dark. However, this phenomenon is reversible and does not mean a malfunction or a display that has been permanently damaged. If the display area is pushed on hard during operation, some graphics will be abnormally displayed but returns to a normal condition after turning off the display once. Even a small amount of condensation on the contact pads (terminals) can cause an electro-chemical reaction which causes missing rows and columns. Give careful attention to avoid condensation.

Storage

Store the display in a dark place where the temperature is 25°C ± 10°C and the humidity below 50%RH. Store the display in a clean environment, free from dust, organic solvents and corrosive gases. Do not crash, shake or jolt the display (including accessories).